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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/643,004	08/21/2000	Garry A. Mercaldi	MI22-1358	8352

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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,004	MERCALDI, GARRY A.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-41 and 47-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *52-59* is/are allowed.

6)☐ Claim(s) *9-14,16-18,20-22,25-35,37-41,47-50,60-63 and 65-69* is/are rejected.

7)☒ Claim(s) *15,19,23,24,36,51 and 64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20051123*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 9-41 and 47-69 is withdrawn in view of the newly discovered reference(s) to Fazan et al. (U.S. 5,597,756) and Nogami et al. (U.S. 6,060,383). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9-14, 16, 17, 18, 20-22, 25-30, 47-50, 62, 63, 65 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan et al. (U.S. 5,597,756) and Nogami et al. (U.S. 6,060,383).

In reference to claims 9-14, 16, 17, 18, 20, 25-30, 37-41, 65, Fazan et al. (Figs.1-2) teach a method of forming a semiconductor device including the steps of providing a substrate (12, 16, 18B), wherein said substrate have a first part (16) and a second part (18B), wherein the first part (16) comprises a dielectric material and said second part (18B) comprises polysilicon; forming a first layer (22, 23) labeled as a nucleation layer comprising silicon nitride and silicon oxide on said first part (16) and said second part (18B) simultaneously; and forming a second layer (24) labeled as deposition layer made of silicon nitride, wherein said first (22, 23) and said second (24) layer are formed by a CVD process (Fazan et al., column 3, lines 37 – 13).

Fazan et al. fail to teach forming said silicon nitride layers using an ALD process. However, Nogami et al. teach a related method of forming nitride layers including forming a silicon nitride layers by either a CVD process and an ALD process (Nogami et al., column 8, lines 20 – 50).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Fazan et al. and Nogami et al. to enable forming the silicon nitride layer of Fazan et al. to be performed according to the teachings of Nogami et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed nitride layer of Fazan et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, since the claimed nucleation layer does not require being directly on the substrate and consisting of one layer having a first part that includes silicon and nitrogen and a second part that includes silicon, nitrogen and oxygen, and the deposition layer directly on the nucleation layer, the combination of Fazan et al. and Nogami et al. reads on the claimed invention, that is, the nucleation layer and the deposition layer is non-selectively deposited on the substrate.

In reference to claim 21, 22 and 50, the combine teachings of Fazan et al. and Nogami et al. fail to teach wherein the nucleation layer comprises less than about 9Å. One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or

are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

In reference to claims 62, 63 and 69, the combined teachings of Fazan et al. and Nogami et al. substantially teach all aspects of the invention but fail to disclose wherein the nucleation layer is CVD deposited at a temperature no greater than about 645°C and at a pressure from about 500mmTorr to about 1.5Torr; and wherein the nucleation layer is ALD deposited at a temperature of 400 to about 550°C and a pressure of 100mmTorr to about 20 Torr. However, the selection of the temperature and pressure conditions is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a desired layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above-mentioned environment conditions to arrive at the claimed invention.

4. Claims 31-35, 37-41, 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan et al. (U.S. 5,597,756), Nogami et al. (U.S. 6,060,383) and Srinivasan et al. (U.S. 5,929,526).

In reference to claims 31-34, 37-41 and 68, Fazan et al. (Figs.1-2) teach a method of forming a semiconductor device including the steps of providing a substrate (12, 16, 18B), wherein said substrate have a first part (16) and a second part (18B), wherein the first part (16) comprises an interlevel dielectric material and said second part (18B) comprises polysilicon; forming a first layer (22, 23) labeled as a nucleation layer comprising silicon nitride and silicon oxide on said first part (16) and said second part (18B) simultaneously; and forming a second layer (24) labeled as deposition layer made of silicon nitride, wherein said first (22, 23) and said second (24) layer are formed by a CVD process (Fazan et al., column 3, lines 37 – 13).

Fazan et al. fail to teach forming said silicon nitride layers using an ALD process. However, Nogami et al. teach a related method of forming nitride layers including forming a silicon nitride layers by either a CVD process and an ALD process (Nogami et al., column 8, lines 20 – 50).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Fazan et al. and Nogami et al. to enable forming the silicon nitride layer of Fazan et al. to be performed according to the teachings of Nogami et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed nitride layer of

Fazan et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, since the claimed nucleation layer does not require being directly on the substrate and consisting of one layer having a first part that includes silicon and nitrogen and a second part that includes silicon, nitrogen and oxygen, and the deposition layer directly on the nucleation layer, the combination of Fazan et al. and Nogami et al. reads on the claimed invention, that is, the nucleation layer and the deposition layer is non-selectively deposited on the substrate.

Still the combined teachings of Fazan et al., Nogami et al. and Srinivasan et al. fail to teach wherein the interlevel dielectric material comprises an oxide material. However, Srinivasan (Fig.2) in a conventional method to form dielectric layers teach forming an interlevel dielectric material made of BPSG (Srinivasan et al., column 1, lines 55 – 67). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Fazan et al. and Nogami et al. with Srinivasan et al. to enable forming the interlevel dielectric layer of Fazan et al. and Nogami et al. according to the teachings of Srinivasan et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed interlevel dielectric layer of Fazan et al. and Nogami et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claims 35, the combined teachings of Fazan et al., Nogami et al. and Srinivasan et al. fail to teach wherein the nucleation layer comprises less than

about 9Å. One of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

In reference to claims 66 and 67, the combined teachings of Fazan et al. and Nogami et al. substantially teach all aspects of the invention but fail to disclose wherein the nucleation layer is CVD deposited at a temperature no greater than about 645°C and at a pressure from about 500mmTorr to about 1.5Torr; and wherein the nucleation layer is ALD deposited at a temperature of 400 to about 550°C and a pressure of 100mmTorr to about 20 Torr. However, the selection of the temperature and pressure conditions is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a desired layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to use the above-mentioned environment conditions to arrive at the claimed invention.

5. Claims 60 and 61 rejected under 35 U.S.C. 103(a) as being unpatentable over Fazan et al. (U.S. 5,597,756) and Nogami et al. (U.S. 6,060,383) as applied to claims 9-14, 16, 17, 18, 20-22, 25-30 and 47-49 above, and further in view of Kim et al. (U.S. 6,500,763 B2).

The combined teachings of Fazan et al. and Nogami et al. teach wherein the first and second layers are used as etch stop layers (Fazan et al., column 3, line 59 – column 4, line 37), but fail to teach wherein said etch stop layer comprise aluminum oxide and tantalum oxide. However, Kim et al. teach a method of forming a semiconductor device including forming depositing etch stop layers comprised of aluminum oxide and tantalum oxide (Kim et al., column 4, lines 1 – 20). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Fazan et al. and Nogami et al. with Kim et al. to enable forming the etch stopping layers of Fazan et al. and Nogami et al. according to the teachings of Kim et al. because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of forming the disclosed etch stop layers of Fazan et al. and Nogami et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Allowable Subject Matter

6. Claims 15, 19, 23, 24, 36, 51, 64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 52-59 are allowed.

Conclusion

8. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
February 3, 2006

George Fourson
Primary Examiner